CLAIMS

1. A method comprising:

analyzing characteristics of signals passing along a first plurality of conductive paths arranged in a first orientation; and

determining a second orientation for a second plurality of conductive paths based on said analyzed characteristics.

2. The method of claim 1, wherein said characteristics comprise timing relationships of signals across said first plurality of conductive paths.

3. The method of claim 2, wherein said timing relationships relate to one of push-out and pull-in of signal timings.

4. The method of claim 1, wherein said first plurality of conductive paths are on a first plane and arranged in said first orientation and said second plurality of conductive paths are on a second plane and arranged in said second orientation.

5. The method of claim 1, wherein said first plurality of conductive paths comprise a first plurality of traces on a first layer of a printed circuit board and said second plurality of conductive paths comprise a second plurality of traces on a second layer of said printed circuit board.

6. The method of claim 5, wherein said first plurality of traces are arranged on said first layer in a first ordered arrangement and said second plurality of traces are arranged on said second

layer in a second ordered arrangement, and determining said second orientation comprises determining said second ordered arrangement based on the analyzed characteristics.

7. The method of claim 1, wherein said first plurality of conductive paths comprise a first plurality of vias coupling a first layer of a printed circuit board to a second layer of said printed circuit board, and said second plurality of conductive paths comprise a second plurality of vias coupling said first layer of said printed circuit board to said second layer of said printed circuit board.

8. A method of designing a printed circuit board comprising:

analyzing at least one characteristic of a first plurality of relatively parallel conductive paths on said printed circuit board, said first plurality of relatively parallel conductive paths being arranged in a pattern in a first area of said printed circuit board; and

rearranging said pattern of conductive paths such that a second plurality of relatively parallel conductive paths in a second area of said printed circuit board have a different geometry with respect to one another as compared to a geometry of said first plurality of relatively parallel conductive paths in said first area.

9. The method of claim 8, wherein said rearranging is based on said analyzed at least one characteristic.

10. The method of claim 8, wherein said at least one characteristic comprises a timing relationship of signals along said first plurality of relatively parallel conductive paths.

11. The method of claim 10, wherein said timing relationship relates to one of push-out and pull-in of signal timings.

12. The method of claim 8, wherein said first plurality of relatively parallel conductive paths are on a first layer of said printed circuit board and said second plurality of relatively parallel conductive paths are on a second plane of said printed circuit board.

13. The method of claim 8, wherein said first plurality of relatively parallel conductive paths comprise a first plurality of traces on a first layer of said printed circuit board and said second plurality of relatively parallel conductive paths comprise a second plurality of traces on a second layer of said printed circuit board.

14. The method of claim 13, wherein said first plurality of traces are arranged on said first layer in a first ordered arrangement and said second plurality of traces are arranged on said second layer in a second ordered arrangement, and rearranging said pattern comprises determining said second ordered arrangement based on said analyzed at least one characteristic.

15. The method of claim 8, wherein said first plurality of relatively parallel conductive paths comprise a first plurality of vias coupling a first layer of said printed circuit board to a second layer of said printed circuit board, and said second plurality of conductive paths comprise a second plurality of vias coupling said first layer of said printed circuit board to said second layer of said printed circuit board.

16. A method comprising:

analyzing a characteristic of a first plurality of conductive paths arranged in a first pattern; and

altering said characteristic by rearranging said pattern.

17. The method of claim 16, wherein said characteristic comprises a timing relationship of signals across said first plurality of conductive paths.

18. The method of claim 17, wherein said timing relationship relates to one of push-out and pull-out of signal timings.

19. The method of claim 16, wherein altering said characteristic comprises determining a second pattern for a second plurality of conductive paths based on said analyzed characteristic.

20. The method of claim 19, wherein said first plurality of conductive paths are on a first plane and arranged in said first pattern and said second plurality of conductive paths are on a second plane and arranged in said second pattern.

21. The method of claim 19, wherein said first plurality of conductive paths comprise a first plurality of traces on a first layer of a printed circuit board and said second plurality of conductive paths comprise a second plurality of traces on a second layer of said printed circuit board.

22. The method of claim 21, wherein said first plurality of traces are arranged on said first layer in a first ordered arrangement and said second plurality of traces are arranged on said second layer in a second ordered arrangement, and altering said characteristic comprises determining said second ordered arrangement based on said analyzed characteristics.

23. The method of claim 19, wherein said first plurality of conductive paths comprise a first plurality of vias coupling a first layer of a printed circuit board to a second layer of said printed circuit board, and said second plurality of conductive paths comprise a second plurality of vias coupling said first layer of said printed circuit board to said second layer of said printed circuit board.